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Attorney Docket No. SEL 163

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF APPEALS AND INTERFERENCES

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| In Re Application of: | Satoshi MURAKAMI et al. |
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| Filed: | March 1, 2000 |
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| Examiner: | Eugene Lee |
| Art Unit: | 2815 |

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## APPEAL BRIEF UNDER 37 C.F.R. 41.37

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## APPEAL BRIEF UNDER 37 C.F.R. §41.37

This Brief is in furtherance of the Notice of Appeal filed in this Application Serial No. 09/610,283 on April 24, 2006 and Notice of Panel Decision from Pre-Appeal Brief Review of June 13, 2006. The time period for filing an appeal brief thereby being reset for July 13, 2006. Accordingly, a two month extension of time and fee are being submitted herewith to extend the period for filing the appeal brief to September 13, 2006.

This appeal is in response to the Final Rejection of January 24, 2006 rejecting all the pending claims.

The claims of the present application are clearly patentable over the cited references, as will be shown *infra*, and Appellant respectfully requests the Board to so rule and allow the application.

## i. STATEMENT OF REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee: Semiconductor Energy Laboratory Co., Ltd., 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan.

## ii. STATEMENT OF RELATED APPEALS AND INTERFERENCES

To the best of Appellant's, Appellant's legal representatives' and Assignee's knowledge, there are no appeals or interferences pending which will affect or be affected by the Board's decision in this appeal.

## iii. STATUS OF CLAIMS

Claims 46-49, 52, 53, 56-79, 81 and 83-145 are pending and rejected. Claims 46-49, 52, 53, 56-79, 81 and 83-145 are the appealed claims and appear *infra* at p. 25 *et seq.*

## iv. STATUS OF AMENDMENTS

No amendment after final has been filed in this application.

## v. SUMMARY OF CLAIMED SUBJECT MATTER

In accordance with §41.37(c)(v), Appellants are providing the following concise explanation of the claimed subject matter. Appellants are providing examples of where each claim element is shown or discussed in the specification and drawings of the present application. These citations are merely examples, as the application has further disclosure of these elements throughout the application.

The dependent claims are based, either directly or indirectly, on one of the independent claims, and accordingly, all the elements listed for the respective independent claims, and the support for these elements in the specification and drawings are as mentioned herein. These dependent claims also add additional elements or limitations which are supported in the specification and drawings.

Independent Claim 46 is directed to a semiconductor device comprising:

a first thin film transistor **(504,701)** formed over an insulating surface, the first thin film transistor comprising **(p. 96, lns. 8-13; Figs. 5C, 28A)**:

a semiconductor film **(306)** comprising crystalline silicon and having at least source **(415)** and drain **(416)** regions and a channel forming region **(413, 414) (p. 25, ln. 22-23; p. 37, lns. 18-21; Fig. 5C)**;

a gate insulating film **(307)** over the channel forming region **(p. 25, ln. 23 - p. 26, ln. 1; Fig. 3A)**; and

a gate electrode **(341)** formed over the gate insulating film **(p. 28, ln. 13-15; Fig. 4B)**;

an interlayer insulating film **(363 or 364)** formed over the first thin film transistor **(p. 30, lns. 3-10; Figs. 5B, 5C)**;

a first conductive layer **(372)** formed over the interlayer insulating film and electrically connected to one of the source and drain regions of the first thin film transistor **(p. 31, lns. 8-10; Fig. 5C)**;

a color filter **(2301)** formed over the interlayer insulating film and the first conductive layer, wherein the color filter covers the entire first thin film transistor **(p. 96, ln. 19 - p. 97, ln. 2; Fig. 28A)**; and

a pixel electrode **(2307)** formed over the color filter and electrically connected to the first conductive layer **(p. 97, ln. 10; Fig. 28A)**.

Independent Claim 47 is directed to a semiconductor device comprising:

a first thin film transistor **(504, 701)** formed over an insulating surface, the first thin film transistor comprising**(p. 96, lns. 8-13; Figs. 5C, 28A)**:

a semiconductor film **(306)** comprising at least a channel forming region **(413, 414) (p. 37, lns. 18-21; Fig. 5C)**;

a gate insulating film **(307)** adjacent to the channel forming region **(p. 25, ln. 23 – p. 26, ln. 1; Fig. 3A)**; and

a gate electrode **(341)** adjacent to the gate insulating film **(p. 28, ln. 13-15; Fig. 4B)**,

an interlayer insulating film **(363 or 364)** formed over the first thin film transistor **(p. 30, lns. 3-10; Figs. 5B, 5C)**;

a first conductive layer **(372)** formed over the interlayer insulating film and electrically

connected to one of source and drain regions **(415, 416)** of the first thin film transistor **(p. 31, lns. 8-10; Fig. 5C)**;

a color filter formed **(2301)** over the interlayer insulating film and the first conductive layer, wherein the color filter covers the entire first thin film transistor **(p. 96, ln. 19 – p. 97, ln. 2; Fig. 28A)**; and

a pixel electrode **(2307)** formed over the color filter and electrically connected to the first conductive layer **(p. 97, ln. 10; Fig. 28A)**.

Independent Claim 48 is directed to a semiconductor device comprising:

a first thin film transistor **(504, 701)** formed over an insulating surface, the first thin film transistor comprising **(p. 96, lns. 8-13; Figs. 5C, 28A)**:

a semiconductor film **(306)** comprising crystalline silicon and having at least source **(415)** and drain **(416)** regions and a channel forming region **(413, 414) (p. 25, ln. 22-23; p. 37, lns. 18-21; Fig. 5C)**;

a gate insulating film **(307)** adjacent to the channel forming region **(p. 25, ln. 23 – p. 26, ln. 1; Fig. 3A)**; and

a gate electrode **(341)** adjacent to the channel forming region with the gate insulating film interposed therebetween **(p. 28, ln. 13-15; Figs. 4B; 5C)**;

an interlayer insulating film **(363)** formed over the first thin film transistor, the interlayer insulating film comprising at least a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide **(p. 31, lns. 8-10; Fig. 5B)**;

a color filter **(2301)** formed over the interlayer insulating film, wherein the color filter covers

the entire first thin film transistor **(p. 96, ln. 19 – p. 97, ln. 2; Fig. 28A)**; and

a pixel electrode **(2307)** formed over the color filter **(p. 97, ln. 10; Fig. 28A)**,

wherein the pixel electrode is electrically connected to the first thin film transistor **(p. 97, ln. 10; Fig. 28A)**.

Independent Claim 52 is directed to a semiconductor device comprising:

a first thin film transistor **(505, 701)** formed over an insulating surface, the first thin film transistor comprising **(p. 96, lns. 8-13; Figs. 5C, 28A)**:

a semiconductor film **(306)** comprising crystalline silicon and having at least source **(415)** and drain **(416)** regions and a channel forming region **(413, 414) (p. 25, ln. 22-23; p. 37, lns. 18-21; Fig. 5C)**;

a gate insulating film **(307)** adjacent to the channel forming region **(p. 25, ln. 23 – p. 26, ln. 1; Fig. 3A)**; and

a gate electrode **(341)** formed adjacent to the channel forming region with the gate insulating film interposed therebetween **(p. 28, ln. 13-15; Figs. 4B, 5C)**;

a first interlayer insulating film **(363 or 364)** formed over the first thin film transistor **(p. 30, lns. 3-10; Figs. 5B, 5C)**;

a first conductive layer **(372)** formed over the first interlayer insulating film and electrically connected to one of the source and drain regions of the first thin film transistor **(p. 31, lns. 8-10; Fig. 5C)**;

a passivation film **(375)** formed over the first conductive layer, the passivation film comprising at least a material selected from the group consisting of silicon nitride, silicon oxide and

nitrated silicon oxide **(p. 96, ln. 8 - p. 97, ln. 1; Fig. 28A)**;

a color filter **(2301)** formed over the passivation film, wherein the color filter covers the entire first thin film transistor **(p. 96, ln. 19 – p. 97, ln. 2; Fig. 28A)**; and

a pixel electrode **(2307)** formed over the color filter and electrically connected to the first conductive layer **(p. 97, ln. 10; Fig. 28A)**.

Independent Claim 56 is directed to a semiconductor device comprising:

a first thin film transistor **(504, 701)** formed over an insulating surface, the first thin film transistor comprising **(p. 96, lns. 8-13; Figs. 5C, 28A)**:

a semiconductor film **(306)** comprising:

a channel forming region **(413, 414) (p. 37, lns. 18-21; Fig. 5C)**; and

a source region **(415)** and a drain region **(416) (p. 37, lns. 18-21; Fig. 5C)**;

a gate insulating film **(307)** over the channel forming region **(p. 25, ln. 23 – p. 26, ln. 1; Fig. 3A)**; and

a gate electrode **(341)** over the gate insulating film **(p. 28, ln. 13-15; Fig. 4B)**;

an interlayer insulating film **(363 or 364)** formed over the first thin film transistor **(p. 30, lns. 3-10; Figs. 5B, 5C)**;

a first conductive layer **(372)** formed over the interlayer insulating film and electrically connected to one of source and drain regions of the first thin film transistor **(p. 31, lns. 8-10; Fig. 5C)**;

a color filter **(2301)** formed over the interlayer insulating film, the first conductive layer and the first thin film transistor, wherein the color filter covers the entire first thin film transistor

**(p. 96, ln. 19 – p. 97, ln. 2; Fig. 28A)**; and

a pixel electrode **(2307)** formed over the color filter and electrically connected to the first conductive layer **(p. 97, ln. 10; Fig. 28A)**.

Independent Claim 57 is directed to a semiconductor device comprising:

a first thin film transistor **(504, 701)** formed over an insulating surface, the first thin film transistor comprising **(p. 96, lns. 8-13; Figs. 5C, 28A)**:

a semiconductor film **(306)** comprising:

a channel forming region **(413, 414) (p. 37, lns. 18-21; Fig. 5C)**; and

a source region **(415)** and a drain region **(416) (p. 37, lns. 18-21; Fig. 5C)**;

a gate insulating film **(307)** adjacent to the channel forming region **(p. 25, ln. 23 – p. 26, ln. 1; Fig. 3A)**; and

a gate electrode **(341)** adjacent to the channel forming region with the gate insulating film interposed therebetween **(p. 28, ln. 13-15; Figs. 4B, 5C)**;

- an interlayer insulating film **(363)** formed over the first thin film transistor, the interlayer insulating film comprising at least a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide **(p. 30, lns. 3-10; Fig. 5B)**;

a color filter **(2301)** formed over the interlayer insulating film and the first thin film transistor, wherein the color filter covers the entire first thin film transistor **(p. 96, ln. 19 – p. 97, ln. 2; Fig. 28A)**; and

a pixel electrode **(2307)** formed over the color filter **(p. 97, ln. 10; Fig. 28A)**.

Independent Claim 58 is directed to a semiconductor device comprising:

a first thin film transistor **(504, 701)** formed over an insulating surface, the first thin film transistor comprising **(p. 96, lns. 8-13; Figs. 5C, 28A)**:

a semiconductor film **(306)** comprising:

a channel forming region **(413, 414) (p. 37, lns. 18-21; Fig. 5C)**; and

a source region **(415)** and a drain region **(416) (p. 37, lns. 18-21; Fig. 5C)**;

a gate insulating film **(307)** adjacent to the channel forming region **(p. 25, ln. 23 – p. 26, ln. 1; Fig. 3A)**; and

a gate electrode **(341)** adjacent to the channel forming region with the gate insulating film interposed therebetween **(p. 28, ln. 13-14; Figs. 4B, 5C)**;

a first interlayer insulating film **( 363 or 364)** formed over the first thin film transistor **(p. 30, ln. 3-10; Figs. 5B, 5C)**;

a first conductive layer **(372)** formed over the first interlayer insulating film and electrically connected to one of the source and drain regions of the first thin film transistor **(p. 31, lns. 8-10; Fig. 5C)**;

a passivation film **(375)** formed over the first conductive layer, the passivation film comprising at least a material selected from the group consisting of silicon nitride and nitrated silicon oxide **(p. 96, ln. 8 – p. 97, ln. 1; Fig. 28A)**;

a color filter **(2301)** formed over the passivation film and the first thin film transistor, wherein the color filter covers the entire first thin film transistor **(p. 96, ln. 19 – p. 97, ln. 2; Fig. 28A)**; and

a pixel electrode **(2307)** formed over the color filter and electrically connected to the first

conductive layer **(p. 97, ln. 10; Fig. 28A)**.

Independent Claim 59 is directed to a semiconductor device comprising:

a first thin film transistor **(504, 701)** comprising **(p. 96, lns. 8-13; Figs. 5C, 28A)**:

a semiconductor film **(306)** comprising at least a channel forming region **(413, 414) (p. 37, lns. 18-21; Fig. 5C)**;

a gate insulating film **(307)** over the channel forming region **(p. 25, ln. 23 - p. 26, ln. 1; Fig. 3A)**; and

a gate electrode **(341)** over the channel forming region with the gate insulating film interposed therebetween **(p. 28, ln. 13-15; Figs. 4B, 5C)**;

an interlayer insulating film **(363 or 364)** formed over the first thin film transistor **(p. 30, lns. 3-10; Figs. 5B, 5C)**;

a first conductive layer **(372)** formed over the interlayer insulating film and electrically connected to one of source and drain regions of the first thin film transistor **(p. 31, lns. 8-10; Fig. 5C)**;

a color filter **(2301)** formed over the interlayer insulating film, the first conductive layer and the first thin film transistor, wherein the color filter covers the entire first thin film transistor **(p. 96, ln. 10 – p. 97, ln. 2; Fig. 28A)**; and

a pixel electrode **(2307)** formed over the color filter and electrically connected to the first conductive layer **(p. 97, ln. 10; Fig. 28A)**.

Independent Claim 60 is directed to a semiconductor device comprising:

a first thin film **(504, 701)** transistor comprising **(p. 96, lns. 8-13; Figs. 5C, 28A)**:

a semiconductor film **(306)** comprising silicon and having at least a channel forming region **(413, 414) (p. 25, ln. 22-23; p. 37, lns. 18-21; Fig. 5C)**;

a gate insulating film **(307)** adjacent to the channel forming region **(p. 25, ln. 23 – p. 26, ln. 1; Fig. 3A)**; and

a gate electrode **(341)** adjacent to the channel forming region with the gate insulating film interposed therebetween **(p. 28, ln. 13-15; Figs. 4B, 5C)**;

an interlayer insulating film **(363)** formed over the first thin film transistor, the interlayer insulating film comprising at least a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide **(p. 30, lns. 3-10; Fig. 5B)**;

a color filter **(2301)** formed over the interlayer insulating film and the first thin film transistor, wherein the color filter covers the entire first thin film transistor **(p. 96, ln. 19 – p. 97, ln. 2; Fig. 28A)**; and

a pixel electrode **(2307)** formed over the color filter **(p. 97, ln. 10; fig. 28A)**.

Independent Claim 61 is directed to a semiconductor device comprising:

a first thin film transistor **(504, 701)** comprising **(p. 96, lns. 8-13; Figs. 5C, 28A)**:

a semiconductor film **(306)** comprising silicon and having at least a channel forming region **(413, 414) (p. 25, ln. 22-23; p. 37, lns. 18-21; Fig. 5C)**;

a gate insulating film **(307)** adjacent to the channel forming region **(p. 25, ln. 23 – p. 26, ln. 1; Fig. 3A)**; and

a gate electrode **(341)** adjacent to the channel forming region with the gate

insulating film interposed therebetween **(p. 28, ln. 13-15; Figs. 4B, 5C)**;

a first interlayer insulating film **(363 or 264)** formed over the first thin film transistor **(p. 30, lns. 3-1; Figs. 5B, 5C)**;

a first conductive layer **(372)** formed over the first interlayer insulating film and electrically connected to one of the source and drain regions of the first thin film transistor **(p. 31, lns. 8-10; Fig. 5C)**;

a passivation film **(375)** formed over the first conductive layer, the passivation film comprising at least a material selected from the group consisting of silicon nitride and nitrated silicon oxide **(p. 96, ln. 8 – p. 97, ln. 1; Fig. 28A)**;

a color filter **(2301)** formed over the passivation film and the first thin film transistor, wherein the color filter covers the entire first thin film transistor **(p. 96, ln. 19 – p. 97, ln 2; Fig. 28A)**; and

a pixel electrode **(2307)** formed over the color filter and electrically connected to the first conductive layer **(p. 97, ln. 10; Fig. 28A)**.

Claims 49 and 53 are dependent on Claims 48 and 52, respectively, and recite that the gate electrode **(341)** is located over the channel forming region **(413, 414) (Fig. 5C)**.

Claims 62-67 are dependent on Claims 56-61, respectively, and recite that the semiconductor film **(306)** comprises crystalline silicon **(p. 25, ln. 22-23)**.

Claims 68-70 are dependent on Claims 46, 48, 52, respectively, and recite that the

semiconductor device further comprises:

a resin film **(2302)** over the color filter **(2301)** **(p. 97, lns. 2-13; Fig. 28A)**;

an electrode **(2303)** over the organic resin film **(p. 97, lns. 2-13; Fig. 28A)**; and

an oxide film **(2304)** of the electrode in direct contact with at least a portion of a surface of the electrode **(p. 97, lns. 2-13; Fig. 28A)**,

wherein the pixel electrode **(2307)** is in direct contact with at least a portion of the oxide film **(Fig. 28A)**, and

wherein a storage capacitor **(2308)** comprises the electrode and the pixel electrode with the oxide film interposed therebetween **(p. 97, lns. 11-13; Fig. 28A)**.

Claims 71-76 are dependent upon Claims 46, 48, 52, 56-58, respectively, and recite that the semiconductor film **(306)** further comprises LDD regions **(417, 418, 419, 420)** between the channel forming region **(413, 414)** and the source and drain regions **(415, 416)** **(p. 37, lns. 17-23; Figs. 5C, 28A)**.

Claims 77-88 are dependent on Claims 46-48, 52, 56-61, respectively, and recite that the semiconductor device further comprises a driver circuit comprising a second thin film transistor **(501, 502 or 503)** **(Fig. 5C)**,

wherein the first thin film transistor **(504; 701)** is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface **(p. 24, lns. 8-10; Fig. 5C)**.

Claims 89-98 are dependent on Claims 46-48, 52, 56-61, respectively, and recite that the semiconductor device is selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a player that uses a recording medium, a camera, a projector, a portable telephone, a portable book and a display device **(p. 100, lns. 2-8; Figs. 25A-25F, 31A-31D, 32A-32C)**.

Claims 99-108 are dependent on Claims 46-48, 52, 56-61, respectively, and recite that said color filter **(2301)** has a flat upper surface **(p. 97, lns. 1-2; Fig. 28A)**.

Claims 109-118 are dependent on Claims 46-48, 52, 56-61, respectively, and recite that said color filter **(2301)** has an opening through which said pixel electrode **(2307)** is electrically connected to the first conductive layer **(372) (p. 97, ln. 10; Fig. 28A)**.

Claims 119-128 are dependent on Claims 46-48, 52, 56-61, respectively, and recite the semiconductor device further comprising one or more gate electrodes **(341)** in addition to the gate electrode **(341) (Fig. 4B)**.

Claims 129-138 are dependent on Claims 46-48, 52, 56-61, respectively, and recite that the gate electrode **(341)** is covered by the interlayer insulating film **(363 or 364)**.

Claims 139-145 are dependent on Claims 109, 110, 112, 113, 115, 116, 118, respectively, and recite the semiconductor device further comprising a second conductive layer **(368)** formed over

the interlayer insulating film **(363 or 364)** and electrically connected to the other of the source **(415)** and drain **(416)** regions of the first thin film transistor **(504, 701) (p. 31, ln. 10; Figs. 5C, 28A)**,

wherein the color filter **(2301)** covers an entire surface of the first conductive layer **(372)** and an entire surface of the second conductive layer except for a part of the first conductive layer overlapping the opening through which the pixel electrode **(2307)** is electrically connected to the first conductive layer **(p. 96, ln. 19 - p. 97, ln. 2; Fig. 28A)**.

## vi. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following are the grounds for rejection presented for review:

A. Claims 46, 47, 59, 65, 89, 90, 96, 99, 100, 106, 109, 110, 116, 139, 140 and 144 are rejected as being unpatentable over Kadota et al. (US 5,818,550) in view of Yanai (US 6,137,552).

B. Claims 48, 49, 52, 53, 60, 61, 66, 67, 91, 92, 97, 98, 101, 102, 107, 108, 111, 112, 117, 118, 141 and 145 are rejected as being unpatentable over Kadota et al. in view of Yanai and further in view of Seo (US 6,323,521).

C. Claims 56, 62, 71, 74, 93, 103, 113 and 142 are rejected as being unpatentable over Kadota et al. in view of Yanai and further in view of Ha (US 5,677,207).

D. Claims 57, 58, 63, 64, 72, 73, 75, 76, 94, 95, 104, 105, 114, 115 and 143 are rejected as being unpatentable over Kadota et al. in view of Yanai in view of Seo and further in view of Ha.

E. Claims 77, 78 and 86 are rejected as being unpatentable over Kadota et al. in view of Yanai and further in view of Matsumoto (US 5,323,042).

F. Claims 79, 81, 87 and 88 are rejected as being unpatentable over Kadota et al. in view of Yanai in view of Seo and further in view of Matsumoto.

G. Claim 68 is rejected as being unpatentable over Kadota et al. in view of Yanai and further in view of Mikoshiba (US 5,499,123).

H. Claims 69 and 70 are rejected as being unpatentable over Kadota et al. in view of Yanai in view of Seo and further in view of Mikoshiba.

I. Claim 83 is rejected as being unpatentable over Kadota et al. in view of Yanai in view of Ha and further in view of Matsumoto.

J. Claims 84 and 85 are rejected as being unpatentable over Kadota et al. in view of Yanai in view of Seo in view of Ha and further in view of Matsumoto.

K. Claims 119, 120 and 126 are rejected as being unpatentable over Kadota et al. in view of Yanai and further in view of Kunii et al. (US 5,412,493).

L. Claims 121, 122, 127 and 128 are rejected as being unpatentable over Kadota et al. in view of Yanai in view of Seo and further in view of Kunii et al.

M. Claim 123 is rejected as being unpatentable over Kadota et al. in view of Yanai in view of Ha and further in view of Kunii et al.

N. Claims 124 and 125 are rejected as being unpatentable over Kadota et al. in view of Yanai in view of Seo in view of Ha and further in view of Kunii et al.

O. Claims 129, 130 and 136 are rejected as being unpatentable over Kadota et al. in view of Yanai further in view of Kadota et al. '512 (US 6,031,512).

P. Claims 131, 132, 137 and 138 are rejected as being unpatentable over Kadota et al. in view of Yanai in view of Seo and further in view of Kadota et al. '512.

Q. Claim 133 is rejected as being unpatentable over Kadota et al. in view of Yanai in view of Ha and further in view of Kadota et al. '512.

R. Claims 134 and 135 are rejected as being unpatentable over Kadota in view of Yanai in view of Seo in view of Ha and further in view of Kadota et al. '512.

## vii. ARGUMENT

### A. BACKGROUND

The present invention is directed to a semiconductor device having a thin film transistor structure. Such a semiconductor device can be used as an electroptical device, such as a liquid crystal display panel, and for electronic equipment with such an electroptical device installed therein as a component.

More specifically, the pending claims of the present application are directed to an embodiment of the semiconductor device wherein, in addition to other features, a color filter is formed over the interlayer insulating film and wherein the color filter covers the entire first thin film transistor. This provides a number of advantages, including the color filter providing a flatting film function. Further, with the claimed structure, the alignment error between the pixel electrode and the color filter nearly disappears,, and therefore a high aperture ratio can be realized. Furthermore, the claimed structure makes it possible for the semiconductor device to be applied to a small panel with a size of 1 inch or less. See e.g. pages 97-98 of the specification of the present application.

Appellant will now address the rejections of the claims in the Final Rejection of January 24, 2006.

### B. THE REJECTIONS OF THE CLAIMS SHOULD BE REVERSED

In the Final Rejection, each of the Examiner's rejections is based on the combination of Kadota (US 5,818,550; hereafter Kadota) and Yanai (US 6,137,552) (and other references).

Appellant respectfully submits that these rejections are improper as a prima facie case of obviousness has not been established and the combination of references is improper.

As explained in MPEP §2142, the burden is initially on the Examiner to establish a prima facie case of obviousness. If the Examiner does not establish a prima facie case, then the rejection is improper and should be withdrawn. To establish a prima facie case of obviousness, there must be some suggestion or motivation to modify or combine references. MPEP §2142 states that:

> "When the motivation to combine the teachings of the references is not immediately apparent, it is the duty of the examiner to explain why the combination of the teachings is proper. *Ex parte Skinner*, 2 USPQ2d 1788 (Bd. Pat. App. & Inter. 1986). A statement of a rejection that includes a large number of rejections must explain with reasonable specificity at least one rejection, otherwise the examiner procedurally fails to establish a *prima facie* case of obviousness. *Ex parte Blanc*, 13 USPQ2d 1383 (Bd. Pat. App. & Inter. 1989)"

As will be explained below, in this case, the Examiner has failed to show a proper motivation to combine Kadota and Yanai to arrive at the claimed invention and the combination of these references is improper.

In particular, each of the pending independent claims of the present application requires a color filter as one element of the claimed semiconductor device and further requires that the color filter cover the entire first thin film transistor.

As the Examiner has admitted in this application, Kadota does not disclose a color filter wherein the color filter covers the entire first thin film transistor. See e.g. page 2 of the Final Rejection of January 24, 2006.

Instead, Kadota discloses color filter 9 divided into discrete segments 9R, 9G and 9B. See e.g. Fig. 1, col. 3, lns. 56-57 and col. 4, lns. 29-30 in Kadota. These discrete segment color filters are

separated from one another and in no way cover the entire TFT (and in fact, if they cover any part of the TFT, it is an extremely small portion, as shown in Fig. 1 in Kadota). From the patent, it is clear that Kadota ***specifically*** designed this structure so that these color filters are separated and not over the TFT. For example, col. 1, lns. 31-40 describe finely dividing the color filter 9 into tiny segments. See also col. 3, lns. 56-57; col. 4, lns. 29-30 in Kadota.

Kadota further states that "*The **critical** feature* of the laminated structure resides in the provision of the third layer between the second and fourth layers." Col. 4, lns. 40-42 (emphasis added). This third layer is planarization film 10 which separates the color filters from the pixel electrodes, protects the color filters against damaging force which may be applied to the color filters in subsequent steps of the manufacturing process, prevents impurities in the color filters from spreading into the liquid crystal, and fills in the concavities and convexities presented by the TFT and the color filters. See e.g. col. 4, lns. 29-47, col. 5, ln. 61 - col,. 6, ln. 3 and col. 7, lns. 36-47 in Kadota. Clearly, in this discrete segmented color filter structure, the planarization film (or third layer) is an important and critical component of the device and disclosure in Kadota and is required to meet the objection of the invention in Kodata (see e.g. col. 2, lns. 17-22 in Kadota).

The Examiner appears to overlook these teachings and criticality in Kadota when combining this reference with Yanai. The Examiner cites Yanai as allegedly disclosing a semiconductor device comprising a color filter which covers a thin film transistor. The Examiner then contends that:

> "it would have been obvious to one of ordinary skill in the art at the time of the invention to have a color filter, wherein the color filter covers the entire first thin film transistor in order to provide a color filter that can adequately emit multiple colors from a thin film transistor" (page 2 of Final Rejection).

This apparently is the Examiner's alleged motivation to combine Kadota and Yanai. There is,

however, no support in the cited references for this alleged motivation as none of the cited references disclose the feature or desire to "provide a color filter that can adequately emit multiple colors from a thin film transistor," nor, as explained below, is there any explanation in the references as to how having a color filter cover the entire first film thin film transistor would meet the Examiner's stated motivation as to provide a color filter that that can adequately emit multiple colors from a thin film transistor (and substitute this for the segmented color filters in Kadota). Further, the Examiner has provided no explanation of where this alleged motivation may be found in the references. Hence, it is not seen how one of ordinary skill in the art reading Kadota would arrive at this alleged motivation and then find the alleged teaching in Yanai of a color filter over the entire TFT to satisfy this motivation. There is simply no reason or suggestion to do so.

As stated in MPEP 2143.01,

> "[o]bviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art." Citing among other cites, *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

The Examiner can only satisfy its burden of establishing a prima facie case of obviousness by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art which would lead the individual to combine the relevant teachings of the references. See *Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1598. The references must suggest the desirability of the combination. MPEP 2143.01, citing *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). To combine references where there is an absence of such teaching or suggestion is to fall victim to hindsight reconstruction which is improper. See *Fine*, 5 USPQ2d at 1599-1600.

Hence, the Examiner has failed to provide the required objective teaching in the art to combine these references. Further, the Examiner cannot rely upon knowledge generally available to one skilled in the art to combine these references.

MPEP 2144.03 states:

> "While "official notice" may be relied on, these circumstances should be rare when an application is under final rejection or action under 37 CFR 1.113. Official notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well-known."

Applicants respectfully submit that the Examiner's statement of motivation is not "capable of instant and unquestionable demonstration as being well-known." MPEP 2144.03 further states that where a statement is not capable of instant and unquestionable demonstration as being well-known or when Applicant challenges a statement as not properly based on common knowledge (as Applicants have done), then "the examiner must provide documentary evidence in the next Office action if the rejection is to be maintained." Accordingly, Applicants respectfully submit that if the Examiner is relying upon alleged knowledge generally available to one skilled in the art to combine these references, then the Examiner needs to withdraw this rejection and provide documentary evidence in support of this reason for combining the references.

Even if the Examiner should provide such evidence, this alleged motivation by the Examiner provides no explanation, reason, or support for use of a color filter that covers the entire first thin film transistor, as recited in the claimed invention. How does one skilled in the art arrive at the idea to have a color filter that covers the entire thin film transistor (TFT) from a desire to provide a color filter that adequately emits multiple colors from the TFT? The claimed feature and the alleged

reason do no appear to be related to one another. Instead, this combination appears to be based on hindsight reconstruction using the claims of the present application as a blue print. As shown in *Fine*, 5 USPQ2d at 1599-1600, such a process is clearly improper.

The Examiner's further comments on page 15 of the Final Rejection confirm that the Examiner has no objective basis for his combination of references and is relying upon alleged general knowledge for which he has no documented basis or support. This section also appears to be another example of hindsight reconstruction.

Hence, there is no proper motivation provided in the Final Rejection for the combination of Kadota and Yanai, and therefore, no prima facie case of obviousness has been established, the combination of references is improper, and all of the §103(a) rejections which are based on this combination are defective. Accordingly, it is respectfully requested that all of the §103(a) rejections be withdrawn.

Claims 139-145

Further, Claims 139-145 recite a second conductive layer formed over the interlayer insulating film and electrically connected to the other of the source and drain regions of the first thin film transistor, wherein the color filter covers an entire surface of the first conductive layer and an entire surface of the second conductive layer except for a part of the first conductive layer overlapping the opening through which the pixel electrode is electrically connected to the first conductive layer.

This feature is not disclosed or suggested by cited references. For example, Yanai discloses the surface of drain electrode 6 partially covered by color filters 9 but also covered by film 10 (not an

opening for pixel electrode as in Claims) 10 and not covered by a single color filter. As the Examiner admits Kadota does not disclose a single color filter that covers the entire first film transistor. The Examiner's arguments on page 15 do not address the specifics of the claim language and what is shown in Yanai.

The Examiner, however, contends in the last paragraph of the section of Response to Arguments that "regarding the applicant's argument on page 28 that Yanai discloses the surface of drain electrode 6 covered by color filters 9 and 10 but not covered by a single color filter, this argument is not persuasive. The color-filter layer of Yanai is a single color filter in the same manner as the applicant's invention. See, for example, Fig. 28A, wherein the applicant discloses the color filter 2301 divided by pixel electrode 2307, however, the color filter is constructed as a single color filter." Appellant respectfully disagrees with the Examiner.

More specifically, as shown in the Summary of the Claimed Subject Matter *supra* and as described in page 96, lines 8-11 of Embodiment 25 of the specification of the present application, the claimed structure is shown in Fig. 28A, which is the same up to the passivation layer as the structure of the semiconductor device of Embodiment 1 (Fig. 3A to 5C). As explained on page 44, lines 10-17 of Embodiment 5 of the specification, Figs. 9A and 9B correspond to the cross sectional structures of Fig. 3A to 5C (Embodiment 1). Therefore, Fig. 9A and 9B can be referred to as top views of Embodiment 25, except for the color filter. On page 45, lines 16-18, the specification of the present application states that "reference numeral 903 denotes a contact area between the drain wiring 372 and the pixel electrode 379." Therefore, the second conductive layer of the claimed invention is only in contact with the pixel electrode through the contact hole represented by the cross of 903. The

contact hole 903 should be opened only at a point corresponding to the contact hole 903, and not divided by the pixel electrode, with the color filter continuously formed in the area around the contact area 903. Therefore, the Examiner's argument is incorrect as the claimed invention (and that taught in the present application) is different than what is shown in Yanai. Hence, the Examiners argument is not persuasive.

Accordingly, Claims 139-145 are not disclosed or suggested by the cited references and are patentable thereover.

Appellant submits that there is clear error in the Examiner's rejections in the Final Rejection of January 24, 2006.

Therefore, the rejection of the claims should be reversed, and the appealed claims allowed.

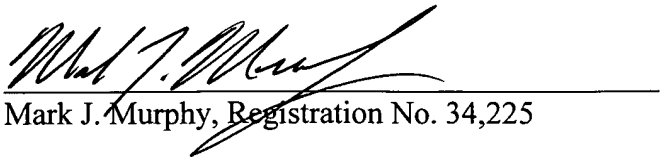
## C. CONCLUSION

For at least the reasons stated above, Appellant earnestly and respectfully submits that the cited references do not render obvious the claims of the present application, and the Examiner's rejections are erroneous and improper.

Hence, the rejection of the claims should be reversed, and the claims allowed.

Accordingly, Appellant requests that this Appeal be sustained in all respects, and that all rejections in the Final Rejection and Advisory Action be reversed.

Respectfully submitted,



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September 12, 2006

## viii. CLAIMS APPENDIX

In accordance with 37 CFR 41.37(c)(1)(viii), the text of the claims on appeal is as follows:

46. A semiconductor device comprising:

a first thin film transistor formed over an insulating surface, the first thin film transistor comprising:

a semiconductor film comprising crystalline silicon and having at least source and drain regions and a channel forming region;

a gate insulating film over the channel forming region; and

a gate electrode formed over the gate insulating film;

an interlayer insulating film formed over the first thin film transistor;

a first conductive layer formed over the interlayer insulating film and electrically connected to one of the source and drain regions of the first thin film transistor;

a color filter formed over the interlayer insulating film and the first conductive layer, wherein the color filter covers the entire first thin film transistor; and

a pixel electrode formed over the color filter and electrically connected to the first conductive layer.

47. A semiconductor device comprising:

a first thin film transistor formed over an insulating surface, the first thin film transistor comprising:

a semiconductor film comprising at least a channel forming region;

a gate insulating film adjacent to the channel forming region; and

a gate electrode adjacent to the gate insulating film,

an interlayer insulating film formed over the first thin film transistor;

a first conductive layer formed over the interlayer insulating film and electrically connected to one of source and drain regions of the first thin film transistor;

a color filter formed over the interlayer insulating film and the first conductive layer, wherein the color filter covers the entire first thin film transistor; and

a pixel electrode formed over the color filter and electrically connected to the first conductive layer.

48. A semiconductor device comprising:

a first thin film transistor formed over an insulating surface, the first thin film transistor comprising:

a semiconductor film comprising crystalline silicon and having at least source and drain regions and a channel forming region;

a gate insulating film adjacent to the channel forming region; and

a gate electrode adjacent to the channel forming region with the gate insulating film interposed therebetween;

an interlayer insulating film formed over the first thin film transistor, the interlayer insulating film comprising at least a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide;

a color filter formed over the interlayer insulating film, wherein the color filter covers the entire first thin film transistor; and

a pixel electrode formed over the color filter,

wherein the pixel electrode is electrically connected to the first thin film transistor.

49. A device according to claim 48, wherein the gate electrode is located over the channel forming region.

52. A semiconductor device comprising:

a first thin film transistor formed over an insulating surface, the first thin film transistor comprising:

a semiconductor film comprising crystalline silicon and having at least source and drain regions and a channel forming region;

a gate insulating film adjacent to the channel forming region; and

a gate electrode formed adjacent to the channel forming region with the gate insulating film interposed therebetween;

a first interlayer insulating film formed over the first thin film transistor;

a first conductive layer formed over the first interlayer insulating film and electrically connected to one of the source and drain regions of the first thin film transistor;

a passivation film formed over the first conductive layer, the passivation film comprising at least a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide;

a color filter formed over the passivation film, wherein the color filter covers the entire first thin film transistor; and

a pixel electrode formed over the color filter and electrically connected to the first conductive layer.

53. A device according to claim 52, wherein the gate electrode is located over the channel forming region.

56. A semiconductor device comprising:

a first thin film transistor formed over an insulating surface, the first thin film transistor comprising:

a semiconductor film comprising:

a channel forming region; and

a source region and a drain region;

a gate insulating film over the channel forming region; and

a gate electrode over the gate insulating film;

an interlayer insulating film formed over the first thin film transistor;

a first conductive layer formed over the interlayer insulating film and electrically connected to one of source and drain regions of the first thin film transistor;

a color filter formed over the interlayer insulating film, the first conductive layer and the first thin film transistor, wherein the color filter covers the entire first thin film transistor; and

a pixel electrode formed over the color filter and electrically connected to the first conductive

layer.

57. A semiconductor device comprising:

a first thin film transistor formed over an insulating surface, the first thin film transistor comprising:

a semiconductor film comprising:

a channel forming region; and

a source region and a drain region;

a gate insulating film adjacent to the channel forming region; and

a gate electrode adjacent to the channel forming region with the gate insulating film interposed therebetween;

an interlayer insulating film formed over the first thin film transistor, the interlayer insulating film comprising at least a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide;

a color filter formed over the interlayer insulating film and the first thin film transistor, wherein the color filter covers the entire first thin film transistor; and

a pixel electrode formed over the color filter.

58. A semiconductor device comprising:

a first thin film transistor formed over an insulating surface, the first thin film transistor comprising:

a semiconductor film comprising:

a channel forming region; and

a source region and a drain region;

a gate insulating film adjacent to the channel forming region; and

a gate electrode adjacent to the channel forming region with the gate insulating film interposed therebetween;

a first interlayer insulating film formed over the first thin film transistor;

a first conductive layer formed over the first interlayer insulating film and electrically connected to one of the source and drain regions of the first thin film transistor;

a passivation film formed over the first conductive layer, the passivation film comprising at least a material selected from the group consisting of silicon nitride and nitrated silicon oxide;

a color filter formed over the passivation film and the first thin film transistor, wherein the color filter covers the entire first thin film transistor; and

a pixel electrode formed over the color filter and electrically connected to the first conductive layer.

59. A semiconductor device comprising:

a first thin film transistor comprising:

a semiconductor film comprising at least a channel forming region;

a gate insulating film over the channel forming region; and

a gate electrode over the channel forming region with the gate insulating film interposed therebetween;

an interlayer insulating film formed over the first thin film transistor;

a first conductive layer formed over the interlayer insulating film and electrically connected to one of source and drain regions of the first thin film transistor;

a color filter formed over the interlayer insulating film, the first conductive layer and the first thin film transistor, wherein the color filter covers the entire first thin film transistor; and

a pixel electrode formed over the color filter and electrically connected to the first conductive layer.

60. A semiconductor device comprising:

a first thin film transistor comprising:

a semiconductor film comprising silicon and having at least a channel forming region;

a gate insulating film adjacent to the channel forming region; and

a gate electrode adjacent to the channel forming region with the gate insulating film interposed therebetween;

an interlayer insulating film formed over the first thin film transistor, the interlayer insulating film comprising at least a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide;

a color filter formed over the interlayer insulating film and the first thin film transistor, wherein the color filter covers the entire first thin film transistor; and

a pixel electrode formed over the color filter.

61. A semiconductor device comprising:

a first thin film transistor comprising:

a semiconductor film comprising silicon and having at least a channel forming region;

a gate insulating film adjacent to the channel forming region; and

a gate electrode adjacent to the channel forming region with the gate insulating film interposed therebetween;

a first interlayer insulating film formed over the first thin film transistor;

a first conductive layer formed over the first interlayer insulating film and electrically connected to one of the source and drain regions of the first thin film transistor;

a passivation film formed over the first conductive layer, the passivation film comprising at least a material selected from the group consisting of silicon nitride and nitrated silicon oxide;

a color filter formed over the passivation film and the first thin film transistor, wherein the color filter covers the entire first thin film transistor; and

a pixel electrode formed over the color filter and electrically connected to the first conductive layer.

62. A device according to claim 56, wherein the semiconductor film comprises crystalline silicon.

63. A device according to claim 57, wherein the semiconductor film comprises crystalline silicon.

64. A device according to claim 58, wherein the semiconductor film comprises crystalline silicon.

65. A device according to claim 59, wherein the semiconductor film comprises crystalline silicon.

66. A device according to claim 60, wherein the semiconductor film comprises crystalline silicon.

67. A device according to claim 61, wherein the semiconductor film comprises crystalline silicon.

68. A device according to claim 46, wherein the semiconductor device further comprising:

a resin film over the color filter;

an electrode over the organic resin film; and

an oxide film of the electrode in direct contact with at least a portion of a surface of the electrode,

wherein the pixel electrode is in direct contact with at least a portion of the oxide film, and

wherein a storage capacitor comprises the electrode and the pixel electrode with the oxide film interposed therebetween.

69. A device according to claim 48, wherein the semiconductor device further comprising:

a resin film over the color filter;

an electrode over the organic resin film; and

an oxide film of the electrode in direct contact with at least a portion of a surface of the electrode,

wherein the pixel electrode is in direct contact with at least a portion of the oxide film, and

wherein a storage capacitor comprises the electrode and the pixel electrode with the oxide film interposed therebetween.

70. A device according to claim 52, wherein the semiconductor device further comprising:

a resin film over the color filter;

an electrode over the organic resin film; and

an oxide film of the electrode in direct contact with at least a portion of a surface of the electrode,

wherein the pixel electrode is in direct contact with at least a portion of the oxide film, and

wherein a storage capacitor comprises the electrode and the pixel electrode with the oxide film interposed therebetween.

71. A device according to claim 46, wherein the semiconductor film further comprises LDD regions between the channel forming region and the source and drain regions.

72. A device according to claim 48, wherein the semiconductor film further comprises LDD

regions between the channel forming region and the source and drain regions.

73. A device according to claim 52, wherein the semiconductor film further comprises LDD regions between the channel forming region and the source and drain regions.

74. A device according to claim 56, wherein the semiconductor film further comprises LDD regions between the channel forming region and the source and drain regions.

75. A device according to claim 57, wherein the semiconductor film further comprises LDD regions between the channel forming region and the source and drain regions.

76. A device according to claim 58, wherein the semiconductor film further comprises LDD regions between the channel forming region and the source and drain regions.

77. A device according to claim 46, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

78. A device according to claim 47, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

79. A device according to claim 48, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

81. A device according to claim 52, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

83. A device according to claim 56, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

84. A device according to claim 57, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

85. A device according to claim 58, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

86. A device according to claim 59, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

87. A device according to claim 60, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

88. A device according to claim 61, further comprising a driver circuit comprising a second thin film transistor,

wherein the first thin film transistor is included in a pixel matrix circuit, and

wherein the pixel matrix circuit and the driver circuit are formed over an insulating surface.

89. A device according to claim 46, wherein the semiconductor device is selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a player that uses a recording medium, a camera, a projector, a portable telephone, a portable book and a display device.

90. A device according to claim 47, wherein the semiconductor device is selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a player that uses a recording medium, a camera, a projector, a portable telephone, a portable book and a display device.

91. A device according to claim 48, wherein the semiconductor device is selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a player that uses a recording medium, a camera, a projector, a portable telephone, a portable book and a display device.

92. A device according to claim 52, wherein the semiconductor device is selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a player that uses a recording medium, a camera, a projector, a portable telephone, a portable book and a display device.

93. A device according to claim 56, wherein the semiconductor device is selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a

player that uses a recording medium, a camera, a projector, a portable telephone, a portable book and a display device.

94. A device according to claim 57, wherein the semiconductor device is selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a player that uses a recording medium, a camera, a projector, a portable telephone, a portable book and a display device.

95. A device according to claim 58, wherein the semiconductor device is selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a player that uses a recording medium, a camera, a projector, a portable telephone, a portable book and a display device.

96. A device according to claim 59, wherein the semiconductor device is selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a player that uses a recording medium, a camera, a projector, a portable telephone, a portable book and a display device.

97. A device according to claim 60, wherein the semiconductor device is selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a player that uses a recording medium, a camera, a projector, a portable telephone, a portable book and a display device.

98. A device according to claim 61, wherein the semiconductor device is selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a player that uses a recording medium, a camera, a projector, a portable telephone, a portable book and a display device.

99. A device according to claim 46 wherein said color filter has a flat upper surface.

100. A device according to claim 47 wherein said color filter has a flat upper surface.

101. A device according to claim 48 wherein said color filter has a flat upper surface.

102. A device according to claim 52 wherein said color filter has a flat upper surface.

103. A device according to claim 56 wherein said color filter has a flat upper surface.

104. A device according to claim 57 wherein said color filter has a flat upper surface.

105. A device according to claim 58 wherein said color filter has a flat upper surface.

106. A device according to claim 59 wherein said color filter has a flat upper surface.

107. A device according to claim 60 wherein said color filter has a flat upper surface.

108. A device according to claim 61 wherein said color filter has a flat upper surface.

109. A device according to claim 46 wherein said color filter has an opening through which said pixel electrode is electrically connected to the first conductive layer.

110. A device according to claim 47 wherein said color filter has an opening through which said pixel electrode is electrically connected to the first conductive layer.

111. A device according to claim 48 wherein said color filter has an opening through which said pixel electrode is electrically connected to the first thin film transistor.

112. A device according to claim 52 wherein said color filter has an opening through which said pixel electrode is electrically connected to the first conductive layer.

113. A device according to claim 56 wherein said color filter has an opening through which said pixel electrode is electrically connected to the first conductive layer.

114. A device according to claim 57 wherein said color filter has an opening through which said pixel electrode is electrically connected to the first thin film transistor.

115. A device according to claim 58 wherein said color filter has an opening through which said pixel electrode is electrically connected to the first conductive layer.

116. A device according to claim 59 wherein said color filter has an opening through which said pixel electrode is electrically connected to the first conductive layer.

117. A device according to claim 60 wherein said color filter has an opening through which said pixel electrode is electrically connected to the thin film transistor.

118. A device according to claim 61 wherein said color filter has an opening through which said pixel electrode is electrically connected to the first conductive layer.

119. A device according to claim 46, further comprising one or more gate electrodes in addition to the gate electrode.

120. A device according to claim 47, further comprising one or more gate electrodes in addition to the gate electrode.

121. A device according to claim 48, further comprising one or more gate electrodes in addition to the gate electrode.

122. A device according to claim 52, further comprising one or more gate electrodes in

addition to the gate electrode.

123. A device according to claim 56, further comprising one or more gate electrodes in addition to the gate electrode.

124. A device according to claim 57, further comprising one or more gate electrodes in addition to the gate electrode.

125. A device according to claim 58, further comprising one or more gate electrodes in addition to the gate electrode.

126. A device according to claim 59, further comprising one or more gate electrodes in addition to the gate electrode.

127. A device according to claim 60, further comprising one or more gate electrodes in addition to the gate electrode.

128. A device according to claim 61, further comprising one or more gate electrodes in addition to the gate electrode.

129. A device according to claim 46, wherein the gate electrode is covered by the interlayer insulating film.

130. A device according to claim 47, wherein the gate electrode is covered by the interlayer insulating film.

131. A device according to claim 48, wherein the gate electrode is covered by the interlayer insulating film.

132. A device according to claim 52, wherein the gate electrode is covered by the interlayer insulating film.

133. A device according to claim 56, wherein the gate electrode is covered by the interlayer insulating film.

134. A device according to claim 57, wherein the gate electrode is covered by the interlayer insulating film.

135. A device according to claim 58, wherein the gate electrode is covered by the interlayer insulating film.

136. A device according to claim 59, wherein the gate electrode is covered by the interlayer insulating film.

137. A device according to claim 60, wherein the gate electrode is covered by the interlayer insulating film.

138. A device according to claim 61, wherein the gate electrode is covered by the interlayer insulating film.

139. A device according to claim 109, further comprising a second conductive layer formed over the interlayer insulating film and electrically connected to the other of the source and drain regions of the first thin film transistor,

wherein the color filter covers an entire surface of the first conductive layer and an entire surface of the second conductive layer except for a part of the first conductive layer overlapping the opening through which the pixel electrode is electrically connected to the first conductive layer.

140. A device according to claim 110, further comprising a second conductive layer formed over the interlayer insulating film and electrically connected to the other of the source and drain regions of the first thin film transistor,

wherein the color filter covers an entire surface of the first conductive layer and an entire surface of the second conductive layer except for a part of the first conductive layer overlapping the opening through which the pixel electrode is electrically connected to the first conductive layer.

141. A device according to claim 112, further comprising a second conductive layer formed over the interlayer insulating film and electrically connected to the other of the source and drain

regions of the first thin film transistor,

wherein the color filter covers an entire surface of the first conductive layer and the second conductive layer except for a part of the first conductive layer overlapping the opening through which the pixel electrode is electrically connected to the first conductive layer.

142. A device according to claim 113, further comprising a second conductive layer formed over the interlayer insulating film and electrically connected to the other of the source and drain regions of the first thin film transistor,

wherein the color filter covers an entire surface of the first conductive layer and an entire surface of the second conductive layer except for a part of the first conductive layer overlapping the opening through which the pixel electrode is electrically connected to the first conductive layer.

143. A device according to claim 115, further comprising a second conductive layer formed over the interlayer insulating film and electrically connected to the other of the source and drain regions of the first thin film transistor,

wherein the color filter covers an entire surface of the first conductive layer and an entire surface of the second conductive layer except for a part of the first conductive layer overlapping the opening through which the pixel electrode is electrically connected to the first conductive layer.

144. A device according to claim 116, further comprising a second conductive layer formed over the interlayer insulating film and electrically connected to the other of the source and drain regions of the first thin film transistor,

wherein the color filter covers an entire surface of the first conductive layer and an entire surface of the second conductive layer except for a part of the first conductive layer overlapping the opening through which the pixel electrode is electrically connected to the first conductive layer.

145. A device according to claim 118, further comprising a second conductive layer formed over the interlayer insulating film and electrically connected to the other of the source and drain regions of the first thin film transistor,

wherein the color filter covers an entire surface of the first conductive layer and an entire surface of the second conductive layer except for a part of the first conductive layer overlapping the opening through which the pixel electrode is electrically connected to the first conductive layer.

## ix. EVIDENCE APPENDIX

None

## x. RELATED PROCEEDINGS APPENDIX

None